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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/452,828	12/01/1999	KENNETH M. BUCKLAND	062891.0373	1800

7590 11/25/2003

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EXAMINER	
ODLAND, DAVID E	
ART UNIT	**PAPER NUMBER**
2662	

DATE MAILED: 11/25/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/452,828	BUCKLAND ET AL.	
	Examiner	Art Unit	
	David Odland	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-35 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-35 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 7-9.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because page 1 shows related applicants but the application numbers of these related applicants have not been provided. Correction is required. See MPEP § 608.01(b).

Claim Objections

2. Claims 27-20 are objected to because of the following informalities: the claims recite dependency on claim 25, but after an inspection of these claims it appear as though they actually depend on claim 26, since they are related to software operations. Note, the claims have been considered as dependent on claim 26 and not claim 25 for the examination related to this Office action. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1,2,4,5,7 and 9-12 and 16-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Koenig et al. (USPN 6,101,198), hereafter known as Koenig.

Referring to claims 1,2,4,5,7 and 9-11, Koenig discloses a time slot interchanger (TSI) for a telecommunications node (a TSI circuit (see figure 4 and claim 1)), comprising an exchange memory (a processor memory (see figure 5 and 10)) including a plurality of exchange memory slots (the processor memory is divided into ODD input, EVEN input and OUTPUT sections (slots) see figures 4,10 and 15 and claim 1)), each exchange memory slot sized to store a traffic channel (the ODD and EVEN buffers each store a frame which comprises 4 T1 signals (see figures 10 and 15 and claim 1)) and including a plurality of discretely addressable fields sized to store a sub-channel (the channels of the T1 signals are stored in entries of the input buffers (see figure 15 and claim 1)), and a controller operable in response to predefined switching instructions (a DSP processor performs the TSI functions according to stored instructions (see figure 5 and claim 1)) to write a sub-channel received in a first time slot to a first field in a memory slot (the DSP writes a T1 channel stored the EVEN input buffer to an entry of the OUTPUT buffer (see figure 15 and claim 14)) and to write a sub-channel received in a second time slot to a second field in the memory slot (the DSP also writes T1 channels that are in the ODD input buffer to the OUTPUT buffer, thus performing TSI functions (see figures 5 and 15 and claim 14));

the controller further operable to read a first sub-channel from a memory slot to an egress time slot and a second sub-channel in the memory slot to a disparate egress time slot (the T1 channels are interchanged (i.e. time slot interchanged) and can read out of the buffer in an output frame such that the time slots from the ODD and EVEN input buffers are not read out of the OUTPUT buffer in the same frame (see figures 4,5,10 and 15 an claim 1 and 14));

the controller further operable to write a sub-channel in a field of a memory slot to a disparate field in a memory slot (the T1 channel written to an entry of one of the ODD or EVEN input buffers can be written to an entry of the OUTPUT buffer (see figure 15 and claim 14));

the controller further operable to write a sub-channel in a field of a memory slot to a disparate field in an egress time slot (the T1 channel written to an entry of one of the ODD or EVEN input buffers can be written to the OUPUT buffer which forms a frame that is transmitted during a time period (see figure 15 and claim 14));

the exchange memory comprising an exchange random access memory (RAM) (the DSP memory can be randomly accessed (see claims 1 and 3)) and an exchange register bank (an OUTPUT buffer (see figures 5 and 15 and claims 1 and 14)), the exchange RAM including a plurality of exchange RAM slots each sized to store the traffic channels (the DSP memory includes the ODD and EVEN input buffers and the OUTPUT buffer which can be considered slots and are sized to each store a frame comprising 4 T1 signals (see figures 4,5,10 and 15 and claims 1 and 14)) and including a plurality of discretely addressable fields sized to store a sub-channel (each of the buffers has entries which are used to store the channels of the T1 signals (see figure 15 and claim 14)) and the exchange register bank including a plurality of exchange registers each sized to store the traffic channel (the OUPUT buffer is sized to store a frame of data (see figure 15)) and including a plurality of discretely addressable fields sized to store a sub-channel (the OUPUT buffer also includes entries which are used to store the channels of the interchanged T1 signals (see figure 15));

the controller further operable to write a first sub-channel in an exchange RAM slot to a first exchange register (the DSP writes an entry of the EVEN input buffer to an entry in the

OUPUT buffer (see figure 15 and claim 14)) and to write a second sub-channel in the exchange RAM slot to a second exchange register (the DSP then writes an entry in the ODD input buffer to the OUPUT buffer (see figure 15 and claim 14));

the controller further operable to write a sub-channel in a field of an exchange RAM slot to a disparate field in an exchange register (the DSP writes an entry from the EVEN input buffer to the OUPUT buffer which is disparate from the ODD input buffer (see figure 15 and claim 14));

the exchange register is internal to the controller (the OUPUT buffer is inside and par tof the DSP (see figures 4 and 5)).

5. Referring to claims 12,16 and 17, Koenig discloses a method for time division multiplex (TDM) switching of traffic in a telecommunications node (a TSI method (see abstract and figures 4 and 5)), comprising receiving a traffic stream including a plurality of traffic channels (a plurality of input signals are received as frames (see figure 10 and 15 and claim 1)) having discrete sub-channels (the frames comprise 4 T1 signals, which comprise 24 channels each (see figures 4 and 5)), writing each traffic channel to a separate memory slot in an exchange memory (each frame is written to either an EVEN input buffer or an ODD input buffer (see figure 15 and claims 1 and 14)), writing a sub-channel in a first memory slot to a first field in a second memory slot (a T1 channel in the EVEN input buffer is written to an entry of an OUTPUT buffer, which can be considered a memory slot (see figure 15 and claims 1 and 14)), writing a sub-channel in a third memory slot to a second field in the second memory slot (a T1 channel in the ODD input buffer is written to an different entry of the OUPUT buffer (see figure 15 and claims 1 and 14))

and reading a combined traffic channel including the sub-channels from the second memory slot to an egress time slot (an interchanged frame is read from the OUTPUT buffer and transmitted during a time period (i.e. a time slot) (see figure 15 and claims 1 and 14));

writing each traffic channel to a separate random access memory (RAM) slot in an exchange RAM (the DSP comprises memory that can be randomly accessed and frames are written to each of the ODD and EVEN input buffers (see figures 10 and 15 and claim 1)), writing a sub-channel in a first RAM slot to a first field in an exchange register of an exchange register bank (a T1 channel written in the EVEN input buffer is written to an entry of the OUTPUT buffer (see figure 15 and claims 1 and 14)) and writing a sub-channel in a second RAM slot to a second field in the exchange register (a T1 channel written in the ODD input buffer is written to another entry of the OUTPUT buffer (see figure 15 and claims 1 and 14));

the exchange register is internal to a controller writing the sub-channels from the RAM slot to the exchange register (the OUTPUT buffer is part of the memory of the DSP (see claim 1)).

6. Referring to claims 18-20, Koenig discloses switch card for a telecommunications node (time slot interchanger in an access bank (see item 20 in figure 4)), comprising a time slot interchanger (TSI) (a TSI DSP circuit (see item 26 in figure 4)), a switch interface operable to receive traffic from a plurality of line cards for the TSI and to transmit traffic from the TSI to the line cards (the mux and demux FPGA interfaces T1 traffic and the TSI (see item 34 of figure 4)), an instruction register operable to provide predefined switching instructions to the TSI for routing traffic to and from the line cards (the DSP uses stored instructions to perform TSI

operations (see claim 1)), an exchange register bank (an output buffer (see figure 10)), an exchange random access memory (RAM) (the DSP has memory, which can be randomly accessed, that comprise an two input buffers that are used for exchanging data (see figure 10 and claim 1)) and the TSI responsive to the predefined switching instructions from the instruction register to write traffic channels received from the switch interface into the exchange RAM (data frames are stored in the memory of the DSP (see figure 10 and 15)), to write a sub-channel in a first slot of exchange RAM to a first field in an exchange register of the exchange register bank (a T1 channel of a T1 signal that is stored in a section (slot) of an EVEN input part of the DSP memory is written to an entry of the output buffer (see figures 10 and 15 and claim 14)) and to write a sub-channel in a second slot of exchange RAM to a second field in the exchange register (a T1 channel of a T1 signal that is stored in a section (slot) of an ODD input part of the DSP memory is written to an entry of the output buffer (see figures 10 and 15 and claim 14));

the TSI further operable to write first and second sub-channels stored in a slot of the exchange RAM to disparate exchange registers (the T1 channels are interchanged by writing the T1 channels into entries of the output buffer (see figures 10 and 15 and claim 14));

the exchange register is internal to the TSI (the output register is part of the memory of the DSP (see claim 1)).

7. Referring to claims 21-25, Koenig discloses a method for processing traffic in a time slot interchanger (TSI) (processing traffic in a TSI circuit (see abstract)) comprising receiving a traffic stream including a plurality of traffic channels (a data stream in received and stored as frames in ODD and EVEN input buffers (see figures 4 and 5 and 15 and claims 1 and 14)),

writing each traffic channel to a memory slot in an exchange memory (each frame is written to either the IDD ort EVEN input buffers, which are part of the memory of a DSP (see figures 4 and 15 and claim 1)), reading a traffic channel stored in a memory slot (a T1 channel stored in the EVEN buffer is read and sent to an OUPUT buffer (see figure 15)), modifying data to generate a modified traffic channel (the time slots of the T1 signals that comprise each frame stored in the ODD and EVEN buffers are interchanged (modified) and a newly interchanged frame is output from the OUPUT buffer (see figure 15 and claim 14)) and writing the modified traffic channel to a memory slot (the interchanged channels are written in the OUPUT buffer (see figure 15 and claim 14));

modifying the data based on logic operations provided with an instruction word for the TSI (the TSI functions are performed by a DSP through the use of stored instructions (see claim 1));

writing the modified traffic channel to a disparate traffic channel (the channels of the T1 signals of the input frames are interchanged and rewritten to a frame which is output from the OUTPUT buffer (see figure 15 and claim 14));

determining a value of the data in the traffic channel and performing a specified action when the data has a specified value (a connection array is used in combination with the instructions to the DSP such that certain T1 channels of the frames are interchanged with others depending on the values of the time slots the channels occupy in the T1 signal and with highway or T1 signal, out of the 4 T1 signals of the frame, they correspond to (see figure 11)).

merging data of the traffic channel with data from a disparate traffic channel to form a conference traffic channel (T1 channels form the frame in the EVEN input buffer are

interchanged with T1 channels from the ODD input buffer to form a combined output frame that in stored in the OUPUT buffer (see figure 15 and claim 14)).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 3,8,13,14,27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koenig in view of Khacherian (USPN 5,768,257), hereafter referred to as Khacherian.

Referring to claims 3,8,13,14,27 and 28, Koenig discloses the system discussed above. Koenig does not disclose that system comprises more than two disparate input buffers and more than one disparate output buffer such that the operations of the claimed limitations could be performed (note, these limitations merely recite operations similar to that of their parent claims except that they use multiple and disparate memories). However, Khacherian discloses a network switching apparatus that includes a plurality of disparate inputs and a plurality of disparate outputs for processing data (se claims 1 and 5). It would have been obvious to one skilled in the art at the time of the invention to configure and implement the Koenig system with more disparate input buffers and plural disparate output buffers, as taught in Khacherian, because if one buffer was to fail other buffers would be available to compensate, thereby making Koenig more reliable. Furthermore, the buffers of Koenig are implemented such that they store only one frame each, thus causing a system bottleneck. Having more of these buffers would improve the

speed and throughput of the Koenig system thus reducing this bottleneck. Furthermore, the Koenig TSI circuit interchanges voice data that has a required level of quality that is to be maintained in order to be properly transported, received and listened to at a receiving node of the network. Therefore, system reliability, throughput and speed of the TSI circuit are particularly important in Koenig. Lastly, Koenig points out, in column 12 lines 23-25, that the TSI circuit could be implemented with any number of input and output buffers, thus strongly suggesting compatibility of the Koenig system with more buffers than that which are exemplified in the drawings and claims.

10. Claims 26,30 and 31-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koenig.

Referring to claims 26,30 and 31-35, Koenig discloses all the limitations recited in these claims, as pointed out in the above corresponding 35 U.S.C. 102(e) rejections of claims 12,16 and 21-15, respectively. However, Koenig does not disclose that the system is implemented in software stored on a computer readable medium. It would have been obvious to one skilled in the art at the time of the invention to implement the Koenig system in this manner because the developmental costs of a software implementation are less than that of a hardware based implementation. Furthermore, software is easier to upgrade than hardware.

11. Claims 6,15 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koenig in view of Willie (USPN 5,883,902), hereafter referred to as Willie.

Referring to claims 6,15 and 29, Koenig discloses the system discussed above. Koenig does not disclose that the traffic channel is a DS-0 and the sub-channel is a 1/4 DS-0. However, Willie discloses a system wherein, ¼ DSO channels of a DSO are time slot interchanged (see column 2 lines 33-53). It would have been obvious to one skilled in the art at the time of the invention to implement this configuration is the Koenig system because such a configuration can be used to support ISDN services, as pointed out by Willie in column 2 lines 33-53. Therefore, this configuration would make Koenig more versatile and flexible by allowing the system to process data that uses the ISDN protocol and support users of the ISDN.

Conclusion

12. The following prior art, which is made of record and not relied upon, is considered pertinent to applicant's disclosure:

a. U.S. Patent Number 6,049,540 to Chrin et al.

b. U.S. Patent Number 4,071,703 to Schaffter et al.

c. U.S. Patent Number 4,228,536 to Gueldenpfennig et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Odland, who can be reached at (703) 305-3231 on Monday – Friday during the hours of 8am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou, can be reached at (703) 305-4744. The fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, who can be reached at (703) 305-4750.

deo

November 19, 2003

JOHN PEZZLO
PRIMARY EXAMINER